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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/495,427	01/31/2000	Tomomichi Nakai	2933SE-88	4844

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EXAMINER	
VILLECCO, JOHN M	

ART UNIT	PAPER NUMBER
2612	6

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/495,427	NAKAI ET AL.	
	Examiner	Art Unit	
	John M. Villecco	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4* is/are rejected.

7)☐ Claim(s) *3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION II

Response to Arguments

1. Applicant's arguments filed May 3, 2004 have been fully considered but they are not persuasive.

2. Regarding claims 1, 2, and 4, the applicant argues that Ito fails to specifically disclose that two clock signals are used to drive a solid-state imaging apparatus or that the clock signal used for vertical transfer has a frequency higher than that of another clock signal used for vertical transferring. However, Suzuki was used to disclose these features. Ito was used to generally show the basic structure employed in an ordinary image sensor in the art at the time the invention was made. Ito shows a light receiving portion (I), a storing portion (S), horizontal transfer portion (D), and horizontal and vertical drive circuits, which Suzuki fails to explicitly disclose.

3. Additionally, applicant argues that Suzuki fails to disclose providing an imaging unit and a read out register unit with two different clock signals or that one clock signal used for vertical transferring has a frequency higher than that of another clock signal used for horizontal transferring. However, as discussed in column 3, line 32 to column 4, line 61 and Figures 4 and 5, Suzuki discloses providing the image unit (IA) and read out register (RA) with two different clock signals. More specifically, as disclosed in Figure 4, clock signal (f1) is applied to the image unit while clock signal (f2) is applied to the readout register. These two clock signals have two different frequencies. Additionally, as shown in Figure 4, Suzuki teaches the clock signal used for vertical transferring has a frequency higher than that of another clock signal used for horizontal transferring as shown when capturing image H1.

4. Furthermore, applicant argues that Watanabe fails to teach that the frequency of the vertical timing signal is higher than that of the horizontal timing signal. However, Watanabe was not used to disclose this feature. Suzuki was used to disclose this feature. Watanabe was used to merely show that it is well known in the art to generate vertical and horizontal transfer timing signals from a constant-cycle reference clock.

5. For the reasons stated above, the rejections from the previous office action will be repeated.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (U.S. Patent No. 5,515,103) in view of Suzuki (U.S. Patent No. 4,686,571) and further in view of Watanabe (U.S. Patent No. 5,731,833).

8. Regarding ***claim 1***, Ito discloses prior art in Figure 1, which includes a solid-state imaging device including a light receiving portion (I), a storing portion (S) adjacent to the light receiving portion (I), and a horizontal transfer portion (D) adjacent to the storing portion (S). Ito also discloses a timing control circuit (6), a vertical drive circuit (2) connecting to the timing control circuit (6) for generating a vertical transfer clock (ϕv), and a horizontal drive circuit consisting of the S and H drivers (3, 4). The horizontal drive circuit generates a horizontal

transfer clock (ϕs) in accordance with the horizontal scan timing signal generated by the timing control circuit.

Ito, however, fails to specifically disclose that the vertical drive circuit generates a vertical transfer clock from a second clock, which is shorter than the first clock, or that the horizontal transfer clock generates a horizontal transfer clock from the first clock. Suzuki, on the other hand, discloses that it is well known in the art to generates drive signals based upon clock signals, which have different times for vertical and horizontal scanning. More specifically, Suzuki discloses varying the imaging and transferring times IA, TA, and RA. In a first cycle imaging (H1) is carried out at high speed using a clock frequency, f1, and transferred through the horizontal register using frequency, f2. The next image, HH1, is captured using a low speed image capture and a high-speed readout. The frequencies of the clocks are determined by the clock signal switching circuit by receiving a clock signal (CK) from the clock signal generating circuit (1). In the first imaging operation (H1) the signals for readout (IA) and transfer (TA) operate using a clock signal with a shorter cycle than the readout (RA). Although not specifically disclosed, it is inherent that the imager of Suzuki would include a timing control circuit, a vertical drive circuit, and a horizontal drive circuit for operating the image sensor. The operation of the imager sensor in Suzuki is performed this way so when the drive signal of the image sensor is lowered, smear is reduced (col. 1, line 66 to column 2, line 2). Therefore, it would have been obvious to one of ordinary skill in the art to modify the imager of Ito to operate in a manner akin to Suzuki's so that smear is reduced.

Additionally, neither Ito nor Suzuki specifically disclose that the timing control signal divides a first clock having a predetermined cycle to generate a vertical and horizontal scan

timing signal. Watanabe, on the other hand, discloses that it is well known in the art to generate vertical and horizontal transfer timing signals (VT, HT) from a constant-cycle reference clock (CK). See column 2, lines 33-46. This serves as a common way to generate vertical and horizontal scanning signals. Therefore, it would have been obvious to one of ordinary skill in the art to generate vertical and horizontal scanning signals from a first clock signal since it serves as a common way of generating timing signals.

9. As for ***claim 2***, Suzuki discloses a dividing circuit (52) disposed in the clock signal switching circuit (5) for dividing the clock signal to generate a generating a first clock by dividing the second clock (CK). In column 4, lines 58-61, Suzuki teaches that the clock (CK) may be directly applied to the gate circuit (53). Therefore, the signals would be generated from the clock signal (CK) as the second clock for generating a vertical clock and signals would be generated from the clock signal generated by the frequency divider (52) for generating a horizontal clock.

10. ***Claim 4*** is considered a method claim corresponding to claim 1. Please see the discussion of claim 1 above.

11. **Claims 1, 2, and 4 can also be rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's own admitted prior art in view of Suzuki (U.S. Patent No. 4,686,571)**.

12. Regarding claim 1, applicant discloses prior art in the specification on pages 1-4, which includes a solid-state image device (1) including a light receiving portion (1a), a storing portion (1b), and a horizontal transfer portion (1c). Also disclosed is a timing control circuit (4) for dividing the clock (MCK) to generate a horizontal timing signal (HD) and a vertical timing

signal (VD), a vertical drive circuit (2) connected to the timing control circuit (4) for generating a vertical transfer clock from the clock signal (MCK), and a horizontal drive circuit (3) for generating a horizontal transfer clock.

Applicant's prior art, however, fails to specifically disclose that the vertical drive circuit generates a vertical transfer clock from a second clock, which is shorter than the first clock, or that the horizontal transfer clock generates a horizontal transfer clock from the first clock. Suzuki, on the other hand, discloses that it is well known in the art to generates drive signals based upon clock signals, which have different times for vertical and horizontal scanning. More specifically, Suzuki discloses varying the imaging and transferring times IA, TA, and RA. In a first cycle imaging (H1) is carried out at high speed using a clock frequency, f1, and transferred through the horizontal register using frequency, f2. The next image, HH1, is captured using a low speed image capture and a high-speed readout. The frequencies of the clocks are determined by the clock signal switching circuit by receiving a clock signal (CK) from the clock signal generating circuit (1). In the first imaging operation (H1) the signals for readout (IA) and transfer (TA) operate using a clock signal with a shorter cycle than the readout (RA). Although not specifically disclosed, it is inherent that the imager of Suzuki would include a timing control circuit, a vertical drive circuit, and a horizontal drive circuit for operating the image sensor. The operation of the imager sensor in Suzuki is performed this way so when the drive signal of the image sensor is lowered, smear is reduced (col. 1, line 66 to column 2, line 2). Therefore, it would have been obvious to one of ordinary skill in the art to modify the imager of the applicant's admitted prior art to operate in a manner akin to Suzuki's so that smear is reduced.

13. As for ***claim 2***, Suzuki discloses a dividing circuit (52) disposed in the clock signal switching circuit (5) for dividing the clock signal to generate a generating a first clock by dividing the second clock (CK). In column 4, lines 58-61, Suzuki teaches that the clock (CK) may be directly applied to the gate circuit (53). Therefore, the signals would be generated from the clock signal (CK) as the second clock for generating a vertical clock and signals would be generated from the clock signal generated by the frequency divider (52) for generating a horizontal clock.

14. ***Claim 4*** is considered a method claim corresponding to claim 1. Please see the discussion of claim 1 above.

Allowable Subject Matter

15. Claims 3 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter: Regarding ***claims 3 and 5***, the primary reason for indication of allowable subject matter is that the prior art fails to teach or reasonably suggest varying the predetermined dividing ratio in accordance with the information charge storage time.

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-6306, (for formal communications; please mark "**EXPEDITED PROCEDURE**"; for informal or draft communications, please label "**PROPOSED**" or "**DRAFT**")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (703) 305-1460. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John M. Villecco
June 17, 2004

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600